CLAIMS

What is claimed is:

1   1.   A processor comprising:

2   a cache having a plurality of hit lines; and

3   a multi-hit detection circuit coupled to the hit lines to detect multiple hits in

4   the cache based on hit signals on the hit lines, and to generate an

5   error flag to indicate if multiple hits have occurred.

1   2.   The processor of claim 1, wherein the cache includes a plurality of

2   comparators coupled to the hit lines to generate the hit signals based on

3   comparisons between cache tags and a lookup tag.

1   3.   The processor of claim 2, wherein the cache includes a multiplexer coupled

2   to the hit lines to select data based on the hit signals.

1   4.   The processor of claim 3, wherein the detection circuit includes a NAND gate

2   having pull-down transistor pairs coupled to the hit lines to pull an output

3   node of the NAND gate low if two different hit signals indicate a hit.

1   5.   The processor of claim 1, wherein the detection circuit includes a NAND gate

2   having pull-down transistor pairs coupled to the hit lines to pull an output

3   node of the NAND gate low if two different hit signals indicate a hit.

1   6.   The processor of claim 5, wherein the detection circuit includes an inverter

2   coupled to the output node to generate the error flag.

1   7.   The processor of claim 5, wherein the cache is a multi-way set associative

2   cache.

1   8.   A circuit comprising:

2   a first comparator coupled to a first way of a set in a cache to compare a

3   first cache tag to be stored in the first way to a lookup tag and to

4   generate a first hit signal on a first hit line;

5   a second comparator coupled to a second way of the set to compare a

6   second cache tag to be stored in the second way to the lookup tag and

7   to generate a second hit signal on a second hit line;

8   a third comparator coupled to a third way of the set to compare a third

9   cache tag to be stored in the third way to the lookup tag and to

10   generate a third hit signal on a third hit line;

11   a first pair of pull-down transistors coupled to the first and second hit lines

12   to pull down an output node if the first and second hit signals both

13   indicate a hit;

14   a second pair of pull-down transistors coupled to the first and third hit

15   lines to pull down the output node if the first and third hit signals both

16   indicate a hit; and

17		a third pair of pull-down transistors coupled to the second and third hit
18		lines to pull down the output node if the second and third hit signals
19		indicate a hit.

1	9.	The circuit of claim 8, further comprising an inverter having an input coupled
2		to the output node, the inverter to provide an error flag at its output node.

1	10.	The circuit of claim 9, further comprising a multiplexer having select inputs
2		coupled to the first, second, and third hit lines, having data inputs to receive
3		data associated with the first, second, and third ways of the set, and having
4		an output to provide selected data.

1	11.	The circuit of claim 10, wherein the error flag indicates the validity of the
2		selected data.

1	12.	The circuit of claim 8, further comprising:
2		at least one additional comparator coupled to an additional way of the set
3		to compare an additional cache tag to be stored in the additional way
4		to the lookup tag and to generate an additional hit signal on an
5		additional hit line; and
6		at least one additional pair of pull-down transistors to pull down the output
7		node if two hit signals both indicate a hit.

1 13.   A method of detecting multi-hit errors in a cache, the method comprising:

2   comparing a plurality of cache tags stored in each of a plurality of ways

3   associated with a indexed set to a lookup tag to generate a plurality of

4   hit signals;

5   selecting selected data from a plurality of memory locations associated

6   with the indexed set based, at least in part, on the plurality of hit

7   signals; and

8   generating an error flag indicating the validity of the selected data by

9   comparing pairs of the plurality of hit signals to determine if any two hit

10   signals both indicate a hit.

1 14.   The method of claim 10, wherein comparing the plurality of cache tags

2   includes comparing four cache tags of a four-way set associative cache to

3   the lookup tag to generate four hit signals.

1 15.   The method of claim 14, wherein generating the error flag includes providing

2   all pairings of the plurality of hit signals to gates of series-coupled pull-down

3   transistor pairs of a NAND gate.

1 16.   The method of claim 13, wherein generating the error flag includes providing

2   pairings of the plurality of hit signals to gates of series-coupled pull-down

3   transistor pairs of a NAND gate.

1   17.   The method of claim 16, wherein generating the error flag further includes

2   inverting an output of the NAND gate.